

We claim:

- 1 1. An apparatus, comprising:
2 write cache storage to store cache lines of write data;
3 a flush dispatcher coupled to the write cache storage to dispatch the cache lines
4 to memory;
5 control logic to:
6 select a first cache line with a first address in the write cache storage for
7 dispatching;
8 determine if a second cache line in the write cache storage has a second
9 address within a predetermined range of the first address; and
10 dispatch the first and second cache lines if the second address is within
11 the predetermined range of the first address.
- 1 2. The apparatus of claim 1, wherein the predetermined range is programmable.
- 1 3. The apparatus of claim 1, wherein control logic to select a first cache line
2 includes logic to select an oldest cache line in the write cache storage.
- 1 4. A method, comprising:
2 receiving a plurality of write requests and storing the plurality of write requests
3 in a plurality of cache lines in a write cache storage;
4 selecting a first one of the plurality of cache lines for dispatching to a memory,
5 wherein the first one of the plurality of cache lines has a first address;

6 determining if a second one of the plurality of cache lines has a second address
7 within a predetermined range of the first address;
8 dispatching the first and second ones of the plurality of cache lines to the
9 memory if the second address is within the predetermined range of the
10 first address; and
11 dispatching the first one but not the second one of the plurality of cache lines to
12 the memory if the second address is not within the predetermined range
13 of the first address.

1 5. The method of claim 4, wherein selecting a first one includes selecting an oldest
2 of the plurality of cache lines.

1 6. The method of claim 4, further comprising programming the predetermined
2 range before selecting.

1 7. A machine-readable medium having stored thereon instructions, which when
2 executed by a processor cause said processor to perform:
3 receiving a plurality of write requests and storing the plurality of write requests
4 in a plurality of cache lines in a write cache storage;
5 selecting a first one of the plurality of cache lines for dispatching to a memory,
6 wherein the first one of the plurality of cache lines has a first address;
7 determining if a second one of the plurality of cache lines has a second address
8 within a predetermined range of the first address;

9 dispatching the first and second ones of the plurality of cache lines to the
10 memory if the first address is within the predetermined range of the
11 second address; and
12 dispatching the first one but not the second one of the plurality of cache lines to
13 the memory if the second address is not within the predetermined range
14 of the first address.

1 8. The medium of claim 7, wherein selecting a first one includes selecting an
2 oldest of the plurality of cache lines.

1 9. The medium of claim 7, further comprising programming the predetermined
2 range before selecting.

1 10. An apparatus, comprising:
2 write cache storage to store cache lines of write data;
3 a flush dispatcher coupled to the write cache storage to dispatch the cache lines
4 to memory;
5 control logic to:
6 dispatch at least one of the cache lines to memory if the number of cache
7 lines in the write cache storage exceeds a first predetermined
8 value; and
9 not dispatch any of the cache lines to memory if the number of cache
10 lines in the write cache storage does not exceed the first
11 predetermined value.

1 11. The apparatus of claim 10, wherein the control logic is further to:
2 dispatch the at least one of the cache lines with a high priority if the number of
3 cache lines in the write cache storage exceeds a second predetermined
4 value higher than the first predetermined value; and
5 dispatch the at least one of the cache lines with a low priority if the number of
6 cache lines in the write cache storage does not exceed the second
7 predetermined value.

1 12. The apparatus of claim 10, wherein the control logic is further to dispatch an
2 oldest one of the cache lines first if the number of cache lines in the write cache storage
3 exceeds the first predetermined value.

1 13. A method, comprising:
2 storing write requests in cache lines of write data in write cache storage;
3 dispatching at least one of the cache lines to memory if the number of cache
4 lines in the write cache storage exceeds a first predetermined value; and
5 not dispatching any of the cache lines to memory if the number of cache lines in
6 the write cache storage does not exceed the first predetermined value.

1 14. The method of claim 13, wherein dispatching further includes:
2 dispatching the at least one of the cache lines with a high priority if the number
3 of cache lines in the write cache storage exceeds a second predetermined
4 value higher than the first predetermined value; and

5 dispatching the at least one of the cache lines with a low priority if the number
6 of cache lines in the write cache storage does not exceed the second
7 predetermined value.

1 15. The method of claim 13, wherein dispatching further includes dispatching an
2 oldest one of the cache lines first if the number of cache lines in the write cache storage
3 exceeds the first predetermined value.

1 16. A machine-readable medium having stored thereon instructions, which when
2 executed by a processor cause said processor to perform:
3 storing write requests in cache lines of write data in write cache storage;
4 dispatching at least one of the cache lines to memory if the number of cache
5 lines in the write cache storage exceeds a first predetermined value; and
6 not dispatching any of the cache lines to memory if the number of cache lines in
7 the write cache storage does not exceed the first predetermined value.

1 17. The medium of claim 16, wherein dispatching further includes:
2 dispatching the at least one of the cache lines with a high priority if the number
3 of cache lines in the write cache storage exceeds a second predetermined
4 value higher than the first predetermined value; and
5 dispatching the at least one of the cache lines with a low priority if the number
6 of cache lines in the write cache storage does not exceed the second
7 predetermined value.

1 18. The medium of claim 16, wherein dispatching further includes dispatching an
2 oldest one of the cache lines first if the number of cache lines in the write cache storage
3 exceeds the first predetermined value.

1 19. An apparatus, comprising:
2 write cache storage to receive a plurality of partial write requests for merging
3 into associated cache lines of write data;
4 a flush dispatcher coupled to the write cache storage to dispatch the cache lines
5 to memory;
6 control logic to:
7 determine if a first cache line associated with a first of the plurality of
8 partial write requests is stored in the write cache storage;
9 if the first cache line is not stored in the write cache storage:
10 retrieve the first cache line from memory;
11 store the retrieved first cache line in the write cache storage; and
12 merge the first of the plurality of partial write requests into the
13 retrieved first cache line.

1 20. The apparatus of claim 19, wherein the control logic is further to merge a
2 second of the plurality of partial write requests into the retrieved first cache line if the
3 retrieved first cache line is associated with the second of the plurality of partial write
4 requests.

1 21. The apparatus of claim 19, wherein the control logic is further to merge the first
2 of the plurality of partial write requests into the first cache line if the first cache line is
3 determined to be stored in the write cache storage.

1 22. A method, comprising:
2 receiving a plurality of partial write requests for merging into associated cache
3 lines of write data in write cache storage;
4 determining if a first cache line associated with a first of the plurality of partial
5 write requests is stored in the write cache storage; and
6 if the first cache line is not stored in the write cache storage:
7 retrieving the first cache line from memory;
8 storing the retrieved first cache line in the write cache storage; and
9 merging the first of the plurality of partial write requests into the
10 retrieved first cache line.

1 23. The method of claim 22, further comprising merging a second of the plurality of
2 partial write requests into the retrieved first cache line if the retrieved first cache line is
3 associated with the second of the plurality of partial write requests.

1 24. The method of claim 22, further comprising merging the first of the plurality of
2 partial write requests into the first cache line if the first cache line is stored in the write
3 cache storage.

1 25. A machine-readable medium having stored thereon instructions, which when
2 executed by a processor cause said processor to perform:

3 receiving a plurality of partial write requests for merging into associated cache
4 lines of write data in write cache storage;
5 determining if a first cache line associated with a first of the plurality of partial
6 write requests is stored in the write cache storage; and
7 if the first cache line is not stored in the write cache storage:
8 retrieving the first cache line from memory;
9 storing the retrieved first cache line in the write cache storage; and
10 merging the first of the plurality of partial write requests into the
11 retrieved first cache line.

1 26. The medium of claim 25, further comprising merging a second of the plurality
2 of partial write requests into the retrieved first cache line if the retrieved first cache line
3 is associated with the second of the plurality of partial write requests.

1 27. The medium of claim 25, further comprising merging the first of the plurality of
2 partial write requests into the first cache line if the first cache line is stored in the write
3 cache storage.

1 28. An apparatus, comprising:
2 write cache storage to receive write requests and to store cache lines of write
3 data;
4 a flush dispatcher coupled to the write cache storage to dispatch the cache lines
5 to memory;
6 control logic to:

7 select a first cache line with a first address in the write cache storage for
8 dispatching;
9 dispatch the first cache line to memory if the number of cache lines in
10 the write cache storage exceeds a first predetermined value;
11 not dispatch any of the cache lines to memory if the number of cache
12 lines in the write cache storage does not exceed the first
13 predetermined value;
14 determine if a second cache line in the write cache storage has a second
15 address within a predetermined range of the first address;
16 dispatch the second cache line if the second address is within the
17 predetermined range of the first address;
18 determine if a third cache line associated with a particular one of a
19 plurality of partial write requests is stored in the write cache
20 storage;
21 if the third cache line is not stored in the write cache storage:
22 retrieve the third cache line from memory;
23 store the retrieved third cache line in the write cache storage; and
24 merge the particular one of the plurality of partial write requests
25 into the retrieved third cache line.

1 29. The apparatus of claim 28, wherein the predetermined range is programmable.

- 1 30. The apparatus of claim 28, wherein the control logic is further to:
2 dispatch the first cache line with a high priority if the number of cache lines in
3 the write cache storage exceeds a second predetermined value higher
4 than the first predetermined value; and
5 dispatch the first cache line with a low priority if the number of cache lines in
6 the write cache storage exceeds the first predetermined value and does
7 not exceed the second predetermined value.